## Remarks

In the present response, two claims (10 and 11) are canceled, and fifteen claims (23-37) are newly presented. Claims 1-9 and 12-37 are presented for examination. Applicant believes that no new matter is entered.

**I. Claim Rejections (Claim 11): 35 USC §112**

Claim 11 is rejected under 35 USC § 112, second paragraph, as being indefinite for lacking antecedent basis for "The data structure" in line 1. Claim 11 is canceled, and the rejection is moot.

**II. Claim Rejections (Claims 10, 11): 35 USC §101**

Claims 10 and 11 are rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. Claims 10 and 11 are canceled, and the rejection is moot.

**III. Claim Rejections (1-3, 5-6, 13-14, 16-17, 20-21): 35 USC § 102**

Claims 1-3, 5-6, 13-14, 16-17, and 20-21 are rejected under 35 USC § 102 as being anticipated by Shephard et al. (USPN 5,633,877, hereinafter Shephard). This rejection is traversed.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Shephard neither teaches nor suggests each element in claims 1-3, 5-6, 13-14, 16-17, and 20-21, these claims are allowable over Shephard.

**Claim 1**

For convenience, claim 1 is reproduced below:

1. A method for chip testing, comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

collecting a set of failure information in response to the testing; and

transmitting the failure information from the chip to the computer over the communications link.

Independent claim 1 recites numerous limitations that are not taught or suggested in Shephard. For example, claim 1 recites "establishing a communications link between a chip and a computer tester." By contrast, Shepard teaches "a programmable ABIST system for testing arrays" (Col. 1, lines 50-51). Figure 1 shows a block diagram of a chip with a memory array and ABIST system, and figures 2 and 3 show block diagrams of embodiments of the ABIST system. (See Col. 2, line 62 to Col. 3, line 3). In short, Shepard is directed to the ABIST system itself. Shepard does not teach a computer or communication link between a computer and the chip and/or the ABIST system on the chip.

As another example, claim 1 recites "collecting a set of failure information ... and transmitting the failure information from the chip to the computer over the communications link." The Office Action cites Col. 2, lines 48-53 for teaching these limitations. This section of Shepard is reproduced below:

> The test data patterns, array address controls, and array write controls are initialized via scanning. The microcode pointer control register thereby controls the various test state machines via the logical test vectors to enable "at speed" functional testing of the array. Test results are gathered via scanning.

This section teaches that the microcode pointer control (see #24 in FIG. 2) of the ABIST system itself controls the test state machines. The test results are then gathered via scanning. Shepard, however, does not teach or suggest that the failure information once collected is transmitted from the chip to the computer over a communication link.

Dependent claims 2-9 depend from claim 1 and thus inherit all the limitations of base claim 1. As such, claims 2-9 are also allowable over Shephard. Further, these dependent claims contain numerous limitations not taught or suggested in Shephard.

**Claim 13**

At least for the reasons given above in connection with claim 1, claim 13 is also allowable over Shephard. Dependent claims 14-19 depend from claim 13 and thus inherit all the limitations of base claim 13. As such, claims 14-19 are also allowable over Shephard. Further, these dependent claims contain numerous limitations not taught or suggested in Shephard.

**Claim 20**

At least for the reasons given above in connection with claim 1, claim 20 is also allowable over Shephard.

**Claim 21**

For convenience, claim 21 is reproduced below:

21. A system for chip testing, comprising:

a communications link;

a computer, operating a set of chip testing software; and

a chip under test coupled to the computer by the communications link, having,

a memory array; and

a Built In Self Test (BIST) module for testing the memory array in response to test algorithms received from the computer and transmitting those addresses within the memory array which failed testing.

Independent claim 21 recites numerous limitations that are not taught or suggested in Shephard. For example, claim 21 recites "a computer, operating a set of chip

testing software." Shepard does not teach or suggest a computer operating chip testing software.

As another example, claim 21 recites "a chip under test coupled to the computer by the communications link." By contrast, Shepard teaches "a programmable ABIST system for testing arrays" (Col. 1, lines 50-51). Figure 1 shows a block diagram of a chip with a memory array and ABIST system, and figures 2 and 3 show block diagrams of embodiments of the ABIST system. (See Col. 2, line 62 to Col. 3, line 3). In short, Shepard is directed to the ABIST system itself. Shepard does not teach a computer or communication link between a computer and the chip and/or the ABIST system on the chip.

As yet another example, claim 21 recites "test algorithms received from the computer and transmitting those addresses within the memory array which failed testing." The Office Action cites Col. 2, lines 48-53 for teaching these limitations. This section of Shepard is reproduced below:

> The test data patterns, array address controls, and array write controls are initialized via scanning. The microcode pointer control register thereby controls the various test state machines via the logical test vectors to enable "at speed" functional testing of the array. Test results are gathered via scanning.

This section teaches that the microcode pointer control (see #24 in FIG. 2) of the ABIST system itself controls the test state machines. The test results are then gathered via scanning. Shepard, however, does not teach or suggest that test algorithms are received from the computer or transmitting addresses which failed testing to the computer.

**IV. Claim Rejections (Claim 10): 35 USC § 102(e)**

Claim 10 is rejected under 35 USC § 102(e) as being anticipated by Bhavsar et al. (USPN 6,408,401 hereinafter Bhavsar). Claim 10 is canceled, and this rejection is moot.

**V. Claim Rejections (Claims 4, 7-8, 12, 15, 18-19, 22): 35 USC § 103(a)**

Claims 4, 7-8, 12, 15, 18-19, and 22 are rejected under 35 USC § 103(a) as being unpatentable over Shephard in view of Bhavsar.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143.

Applicant asserts that the rejection does not satisfy these criteria. For example, the cited art does not teach or suggest each and every limitation of the claims.

**Claim 12**

For convenience, claim 12 is reproduced below:

12. A method for chip testing, comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing a memory array within the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

adding an address under test and those bit locations which failed to a set of failed address information, if a set of data written to the address under test is not equivalent to a set of data read-out from the address under test;

transmitting the failed address information from the chip to the computer over the communications link; and

generating a bit-map on the computer, from the failed address information, of the failed bit locations within the memory array.

Independent claim 12 recites numerous limitations that are not taught or suggested, alone or in combination, in Shephard and Bhavsar. For example, claim 12

recites "establishing a communications link between a chip and a computer tester." Claim 12 also recites "receiving on the chip an initial test algorithm over a communication link." By contrast, Shepard teaches "a programmable ABIST system for testing arrays" (Col. 1, lines 50-51). Figure 1 shows a block diagram of a chip with a memory array and ABIST system, and figures 2 and 3 show block diagrams of embodiments of the ABIST system. (See Col. 2, line 62 to Col. 3, line 3). In short, Shepard is directed to the ABIST system itself. Shepard does not teach a computer or communication link between a computer and the chip and/or the ABIST system on the chip.

As another example, claim 1 recites "transmitting the failed address information from the chip to the computer over the communications link." The Office Action cites Col. 2, lines 48-53 for teaching these limitations. This section of Shepard is reproduced below:

> The test data patterns, array address controls, and array write controls are initialized via scanning. The microcode pointer control register thereby controls the various test state machines via the logical test vectors to enable "at speed" functional testing of the array. Test results are gathered via scanning.

This section teaches that the microcode pointer control (see #24 in FIG. 2) of the ABIST system itself controls the test state machines. The test results are then gathered via scanning. Shepard, however, does not teach or suggest that the failed address information once collected is transmitted from the chip to the computer over a communication link.

As yet another example, claim 12 recites "generating a bit-map on the computer, from the failed address information, of the failed bit locations within the memory array." In response, the Office Actions states: "Shephard does not teach the generating a bit-map from the failure information of failed bit locations within the memory array or adding failed bit locations of the failed address." Applicant agrees. The Office Action, however, attempts to cure this deficiency with the addition of Bhavsar. The Office Action cites Col. 4, lines 30-32 of Bhavsar. This section is reproduced below:

> The test system 15 applies test stimuli via wafer probe 13, and generates a fault-bitmap for each chip, which is off-loaded to the test system.

Applicant respectfully disagrees with the conclusion of the Office Action. This section of Bhavsar is discussing prior, typical manufacturing of wafers before the wafers are cut. Bhavsar itself is directed to chips having, on the chip itself, logic for performing a self-test and self-repair algorithm (see Col. 4, lines 13-15). FIG. 2 of Bhavsar shows the test and repair logic circuit 201 that is embedded in the chip and includes the BIST (see Col. 4, lines 47-54). Thus, the chip itself in Bhavsar performs both self-test and self-repair. By contrast, claim 12 recites "generating a bit-map on the computer." In other words, Applicant claims transmitting the failed address information from the chip to the computer. The computer then generates the bit-map. Again, Bhavsar teaches and suggests generating and repairing on the chip itself.

Dependent claims 4 and 7-8 depend from claim 1 and thus inherit all the limitations of base claim 1. As such, for at least the reasons given in connection with claim 1 in Section III, these dependent claims are allowable over Shephard and Bhavsar.

Dependent claims 15 and 18-19 depend from claim 13 and thus inherit all the limitations of base claim 13. As such, for at least the reasons given in connection with claim 13 in Section III, these dependent claims are allowable over Shephard and Bhavsar.

Dependent claim 22 depends from claim 21 and thus inherits all the limitations of base claim 21 in Section III. As such, for at least the reasons given in connection with claim 21, this dependent claim is allowable over Shephard and Bhavsar.

**VI. Claim Rejections (Claim 9): 35 USC § 103(a)**

Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over Shephard in view of Bosse (USPN 4,586,178, hereinafter Bosse). Applicant respectfully traverses.

Dependent claim 9 depends from claim 1 and thus inherits all the limitations of base claim 1. As such, for at least the reasons given in connection with claim 1 in Section III, this dependent claim is allowable over Shephard and Bosse.

**VII. Claim Rejections (Claim 11): 35 USC § 103(a)**

Claim 11 is rejected under 35 USC § 103(a) as being unpatentable over Bhavsar in view of Orita et al. (USPN 6,499,119, hereinafter Orita). Claim 11 is canceled, and this rejection is moot.

**VIII. New Claims**

Applicant submits new claims 23-37. These claims recite numerous limitations that are not taught or suggested, alone or in combination, by the art of record.

**CONCLUSION**

In view of the above, Applicant believes claims 1-9 and 12-37 are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. (281) 514-8236, Facsimile No. (281) 514-8332. In addition, all correspondence should continue to be directed to the following address:

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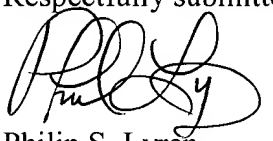
Respectfully submitted,



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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 3rd day of June, 2004.

By Be Henry
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